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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,164	03/03/2004	David A. Knol	HDI-001	3762

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,164	KNOL ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-9 and 14-16* is/are rejected.

7)☒ Claim(s) *3-6,10-13 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/04,5/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1-20 is objected to because of the following informalities:

1. Claim 7, line 18 replace "D)" with – E) --.

2. Claim 7, line 21 replace "E)" with – F) --.

3. Claim 7, line 24 replace "F)" with – G) --.

4. In all claims and Abstract replace "physical block" with – physical block--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 7-9 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ginetti et al. (US Patent 6,170,080).

6. As to claims 1, 7 and 14 Ginetti discloses:

(1), (14) A method/circuit design software of operating a computer to provide a floor planning tool to an integrated circuit designer, comprising the steps (col.2, ll.12-16; col.3, ll.63-67; col.4, ll.1-4; col.16, ll.27-28):

A) storing the data structures of a logical netlist (logical cells) (col.9, ll.56-65; col.11, ll.36-48);

B) displaying on one portion of a computer display a representation of

the instances (logical hierarchy) defined by said logical netlist (col.3, ll.63-67; col.4, ll.54-59; col.5, ll.17-25);

C) providing one or more tools a user can invoke to create and locate physical blocks on a floorplan (physical hierarchy) of an integrated circuit being designed (col.3, ll.49-58; col.3, ll.63-67; col.4, ll.1-4), said floor plan comprising one or more which may be nested ("One goal of a Register Transfer Level floorplanner according to an exemplary embodiment of the present invention is to be able to represent both the original logical hierarchy and the physical hierarchy in order to help the designer easily move through the representations", col.4, ll.54-65) to establish a physical hierarchy (col.5, ll.14-16; col.5, ll.21-23), and responding to invocation of one or more of said tools by creating one or more said physical blocks (col.5, ll.14-16), each physical block represented by a data object having a predetermined structure (col.4, ll.9-12; col.4, ll.18-21), said floorplan being displayed on the same computer display (col.4, ll.65-66) as said representation of said instances defined by said logical netlist;

D) providing one or more tools (computer tools such as keyboard, mouse, display etc.) a user can invoke to assign instances from said displayed representation of instances defined by said logical netlist into physical blocks in said displayed hierarchy of physical blocks (one-to-one mapping/switch command) (col.5, ll.47-56; col.5, ll.65-67; col.6, ll.1-9; col.9, ll.12-15; col.9, ll.66-67; col.10, ll.1-15);

E) responding to such assignment operations by changing the data in said data objects representing said physical blocks to reflect which instances are

assigned to each physical block (col.5, ll.57-67; col.6, ll.1-9; col.9, ll.12-15; col.9, ll.66-67; col.12, ll.42-49); and

F) further responding to such assignment operations by determining the original connectivity between instances defined in said logical netlist and automatically changing data in predetermined data objects of said physical hierarchy so as to recreate said original connectivity by creating new nets and new pins as necessary which recreate said original connectivity (col.10, ll.16-35; col.13, ll.45- 58; col.14, ll.49-65);

(7) An apparatus comprising:

a computer display (col.3, ll.63-67);

a keyboard and pointing device (col.4, ll.1-4);

a computer coupled to said display, keyboard and pointing device, and programmed to perform the following functions (col.3, ll.63-67; col.4, ll.1-4):

A) storing the data structures of a logical netlist (logical cells) (col.9, ll.56-65; col.11, ll.36-48);

B) displaying on one portion of a computer display a representation of the instances (logical hierarchy) defined by said logical netlist (col.3, ll.63-67; col.4, ll.54-59; col.5, ll.17-25);

C) providing one or more tools a user can invoke to create and locate physical blocks on a floorplan (physical hierarchy) of an integrated circuit being designed (col.3, ll.49-58; col.3, ll.63-67; col.4, ll.1-4), said floor plan comprising one or more which may be nested ("One goal of a Register Transfer Level floorplanner

according to an exemplary embodiment of the present invention is to be able to represent both the original logical hierarchy and the physical hierarchy in order to help the designer easily move through the representations", col.4, ll.54-65) to establish a physical hierarchy (col.5, ll.14-16; col.5, ll.21-23), and responding to invocation of one or more of said tools by creating one or more said physical blocks (col.5, ll.14-16), each physical block represented by a data object having a predetermined structure (col.4, ll.9-12; col.4, ll.18-21), said floorplan being displayed on the same computer display (col.4, ll.65-66) as said representation of said instances defined by said logical netlist;

D) providing one or more tools (computer tools such as keyboard, mouse, display etc.) a user can invoke to assign instances from said displayed representation of instances defined by said logical netlist into physical blocks in said displayed hierarchy of physical blocks (one-to-one mapping/switch command) (col.5, ll.47-56; col.5, ll.65-67; col.6, ll.1-9; col.9, ll.12-15; col.9, ll.66-67; col.10, ll.1-15);

E) responding to such assignment operations by changing the data in said data objects representing said physical blocks to reflect which instances are assigned to each physical block (col.5, ll.57-67; col.6, ll.1-9; col.9, ll.12-15; col.9, ll.66-67; col.12, ll.42-49); and

F) further responding to such assignment operations by determining the original connectivity between instances defined in said logical netlist and automatically changing data in predetermined data objects of said physical hierarchy so as to recreate said original connectivity by creating new nets and

new pins as necessary which recreate said original connectivity (col.10, ll.16-35; col.13, ll.45- 58; col.14, ll.49-65).

7. As to claims 2, 8-9 and 15-16 Ginetti recites:

(2), (8)- (9), (15)-(16) The method/apparatus/software, wherein said assignment operations comprise selecting and dragging instances from the displayed logical hierarchy into displayed physical (col.5, ll.47-64; col.5, ll.65-67; col.6, ll.1-9; col.9, ll.66-67; col.10, ll.1-15; col.12, ll.20-38).

Allowable Subject Matter

8. Claims 3-6, 10-13 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method/apparatus/circuit design software of operating a computer to provide a floor planning tool to an integrated circuit designer, wherein step E comprises the steps: marking instToAppend entries designating instances from said logical netlist which have been moved to a physical block with a pointer to the physical block to each instance has been moved, said pointer being in an array m_instanceAssignments (hereafter referred to as the array) which defines which instances are assigned to each physical block; marking all child instances in said logical hierarchy of each said instToAppend in said array to point to the same physical block to which said instToAppend was assigned;

recursing up the logical hierarchy from instToAppend until a rooted parent is found which has been assigned to a physical block (hereafter called rootedpBlock) and mark the rooted parent as zero in said array, where a rooted parent is an instance which is defined by a data object in said physical hierarchy which has a flag set which indicated said rooted parent has been assigned to a physical block and where marking an instance to zero in said array causes said instance to disappear from the physical hierarchy, where disappear from the physical hierarchy means the instance is not assigned to a particular physical block; unwinding the recursion from said rooted parent along a line of said physical hierarchy toward said instToAppend and mark as zero in said array all ancestor instances in said physical hierarchy between said rooted parent and said instToAppend, where an ancestor instance is any instance in said physical hierarchy on a line of descendants between said rooted parent and said instToAppend not including either said rooted parent nor said instToAppend; marking all siblings of any ancestor instance in said array as assigned to said rooted physical block if not already so marked by setting a flag in a data structure representing said instance in said physical hierarchy to a "rooted" state and making sure a pointer to said sibling is present in a data structure representing said rooted physical block in said physical hierarchy, determining if all sibling instances of said instToAppend in said physical hierarchy are marked as belonging to the same physical block as said instToAppend, and, if so, performing a collapse operation to resurrect a parent instance of said siblings in said physical hierarchy by removing or setting to zero entries in said array for all said sibling instances which are components of said parent instance and adding an entry to

said array for said parent instance and data indicating said parent instance is assigned to the same physical block as said sibling instances which were component instances of said parent instance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

Thuan Do
Primary examiner.
09/26/2005